POWER PERFORMANCE OF THERMALLY-SHUNTED HETEROJUNCTION BIPOLAR TRANSISTORS

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ABSTRACT

The effects of layout and thermal shunt configuration on output power, efficiency, and gain of thermally-shunted AlGaAs/GaAs HBT's were investigated. A maximum power density of 16 mW/μm^2 at 10 GHz (CW) was observed. The power gain and power-added efficiency (PAE) at this power density were 7.8 dB and 65%, respectively.

INTRODUCTION

The purpose of this work was to extend the power performance of thermally-shunted AlGaAs/GaAs heterojunction bipolar transistors (HBT's). The research investigated the effects of device layout and thermal shunt configuration on output power, efficiency, and gain. The results produced a significant advancement in the state-of-the-art and showed that smaller emitter diameters were better. A maximum power density of 16 mW/μm^2 at 10 GHz (CW) was observed with an output power of 760 mW. The power gain and power-added efficiency (PAE) at this power density were 7.8 dB and 65%, respectively. This is the highest reported power density for HBT's, and it exceeds the previously reported maximum power densities by 60% [1,2].

Many aspects of this work are original and significant. These are the first reported results on the effects of alternative emitter layout geometries and thermal shunt design on the large-signal power performance of HBT's. This unique work is significant for microwave circuit and device engineers for many reasons. Power density and efficiency are important device parameters which can constrain the application of HBT's. Device impedance generally scales inversely with the active area, and low device impedance complicates the design of power matching networks at high frequency, such as limiting the amplifier's gain-bandwidth product. Therefore, since the active area should be minimized, increased power densities are required. High efficiency is required to minimize the total dissipated power. This yields increased battery lifetime and larger arrays of power sources. High efficiency also minimizes the junction temperature and reduces adverse thermal effects, such as decreased gain and reduced reliability. Finally, the magnitudes of the observed power densities are significant. These results (as well as [1] and [2]) clearly exceed the commonly accepted power limitation [3, 4] of HBT's.

POWER CHARACTERIZATION

The investigation used AlGaAs/GaAs HBT's with 1-μm thick collectors and a collector doping density of 10^{16} cm^{-3}, as well as with 0.7-μm thick collectors and a collector doping density of 5×10^{16} cm^{-3}. The devices were fabricated using a thermal shunt process [5]. The collector-base breakdown voltages were 30 V and 17 V, respectively. The emitter layouts consisted of the following two types: (1) an array of circular dots within a rectangular base finger, and (2) conventional rectangular emitters within a rectangular base finger. Devices with nominal total emitter area of 80-, 150-, and 200-μm^2 were used. A thick thermal shunt was used to electrically and thermally ground the emitters in a common-emitter configuration, and the devices were probed on-wafer. The substrates were

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approximately 625-μm thick. The device layout is illustrated in Figure 1, and a cross-sectional view of the structure is depicted in Figure 2.

Power characterization at 10 GHz was completed using Maury Microwave's load pull system and standard power measurement techniques. An example of typical results for two alternative circular emitters is shown in Figure 3. To verify the results, independent power measurements were completed on a representative HBT at another facility using Focus Microwave, Inc.'s load pull system. The results agreed within 0.1 dB.

The characterization used two approaches. The first approach compared alternative designs with respect to performance. The second approach established the maximum power density of a given device. While the first approach required consistent bias conditions for purposes of comparisons, the second approach used variable bias conditions.

The first approach maintained a moderate collector supply voltage of 6 V to prevent the various devices from burning-out when the rf source was switched on and off at high power levels during iterative load and source pull procedures. The rf input power was sufficient to force the devices into 1-dB compression during optimization. Once the match was optimized, the input power was swept to drive the output power from linear to saturated values.

Using the first approach, devices of the same emitter area, but differing layouts were compared from the same wafer. The circular emitters exhibited greater output power at peak PAE than rectangular emitters. This result is shown in Figure 4 for the case of 80-μm^2 emitters. The output power at peak PAE (Figures 4, 5, and 6) was similar for all the devices with a constant moderate collector bias and equivalent emitter layout (circular or rectangular), since the output match did not vary greatly and the collector bias voltage was limiting the power.

However, the peak PAE varied significantly. For example, Figure 5 shows that the power performance of devices with circular emitters improved with increasing periphery-to-area ratio. The comparison shown in Figure 5 was made using devices with a nominal total emitter area of 80 μm^2 and a fixed collector bias of 6 V and 40 kA/cm^2. As shown in Figure 6, increasing finger separation yielded substantial improvements in the PAE with constant dc-bias conditions. The zero-separation device shown in Figure 6 consisted of a single, large emitter dot. This device would be expected to exhibit the greatest thermal resistance and the lowest emitter utilization of the devices in this set of measurements. This set consisted of devices with a nominal total emitter area of 200 μm^2 and a constant base bias of 2.5 kA/cm^2.

An equivalent result was obtained when only the thermal shunt thickness was varied. This is consistent with decreasing the effective thermal impedance of the devices [6]. This result is shown in Figure 7 for devices with a fixed finger separation. These devices had a nominal emitter area of 200 μm^2 and a constant base bias of 2.5 kA/cm^2.

The maximum power density was determined using the second characterization approach. The second approach used a fixed source and load match determined from the first approach. As the available power and the collector voltage were increased, the base current was adjusted to maintain the gain and PAE.

The greatest power density was obtained from devices with the smallest diameter and which yielded the greatest PAE from the first approach. The circular devices were used in the second approach since they generally exhibited greater PAE. The collector supply was varied up to 15 V for devices with a 30-V collector-base breakdown voltage.

An output power of greater than 760 mW was obtained from devices with a nominal emitter diameter of 2 μm. However, only 400 mW was obtained from devices with an emitter diameter of 5 μm and same total emitter area. The 2-μm diameter devices yielded a record power density of 16 $mW/\mu m^2$ at 10 GHz (CW). The power gain and PAE at this power density were 7.8 dB and 65%, respectively. Even without considering the undercut of the emitter metallization due to the wet chemical etch, the nominal power density of 9.55 $mW/\mu m^2$ exceeds previous reported values. The estimated undercut of 0.23 μm is consistent with the emitter's semiconductor thickness of 0.3 μm, and was verified with electrical, focused-ion beam, and SEM analysis as shown in Figure 8.

The combination of thermal management and layout provided the observed enhancements in power performance. A thermal shunt avoided the use of ballast resistance. By minimizing the parasitic resistance, a greater efficiency was

possible. Hence, the lower dissipation led to lower junction temperatures. By increasing the periphery-to-area ratio (P/A), the efficiency and output power were increased, as well. Also, the thermal shunt thickness affected the performance by reducing the thermal resistance.

The large P/A and low thermal impedance ensured a uniform junction temperature. The combination of high efficiency and uniform temperature with the inherently high electrical emitter utilization of HBT's made the formation of localized hot spots and localized high current densities less likely to occur. By suppressing the formation of small regions with hot spots and high current densities, the output power of the device can be maximized since filaments are less likely to form. Additionally, as the devices enter saturated power conditions, the voltage and current waveforms transition from cosinusoidal to trapezoidal pulse trains, and the output capacitance increases and becomes nonlinear. These effects led to a substantial increase in saturated output power at peak PAE greater than the maximum linear output power.

CONCLUSION

The effects of layout and thermal shunt configuration were examined using standard power measurement techniques. Various devices were measured and the power performance improved with increasing periphery-to-area ratio and increasing finger separation. Also, for a given emitter area, the circular emitters exhibited superior peak PAE and power as compared to rectangular emitters. A record power density of 16 mW/μm^2 at 10 GHz (CW) was observed. The power gain and PAE at this power density were 7.8 dB and 65%, respectively.

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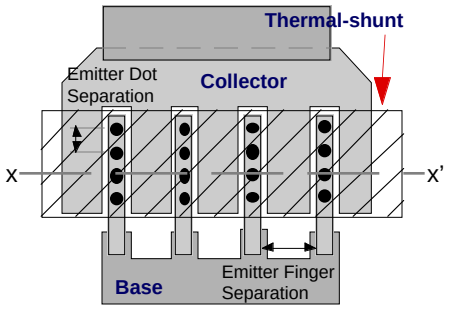

Figure 1. Basic layout of devices.

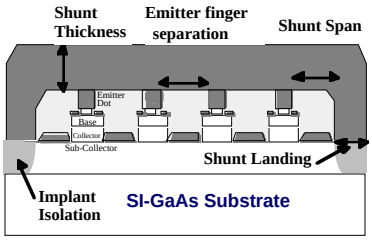

Figure 2. Cross-sectional view of layout. Viewed at the XX' cut-plane in Figure 1.

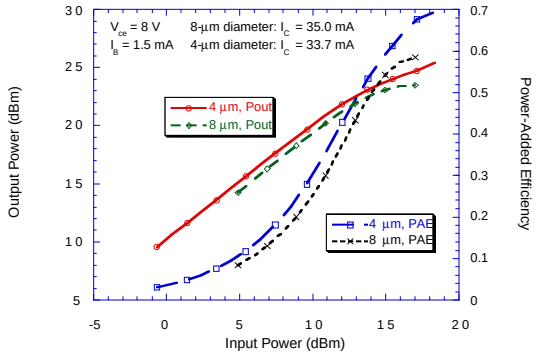

Figure 3. Typical swept power results at 10 GHz for circular emitter diameters of 4 and 8 µm. The total active area was 150 µm^2.

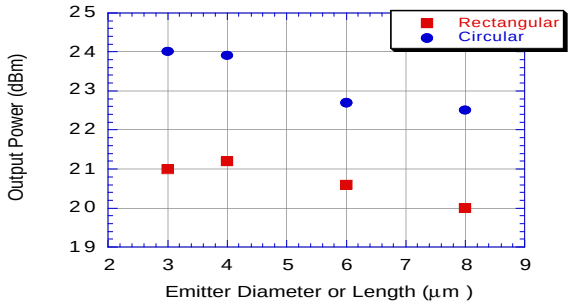

Figure 4. Comparison of output power at peak power-added efficiency for circular and rectangular emitters of 80 µm^2.

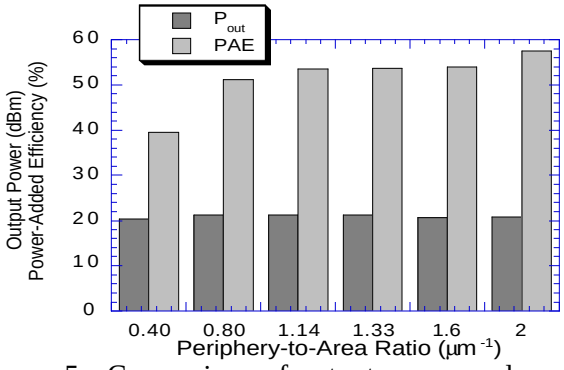

Figure 5. Comparison of output power and power-added efficiency as a function of periphery-to-area ratio.

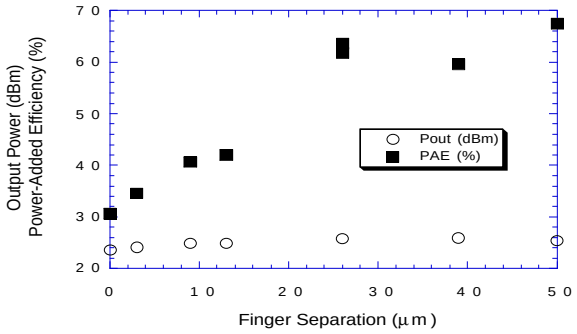

Figure 6. Comparison of output power at peak power-added efficiency (PAE) and PAE as a function of finger spacing.

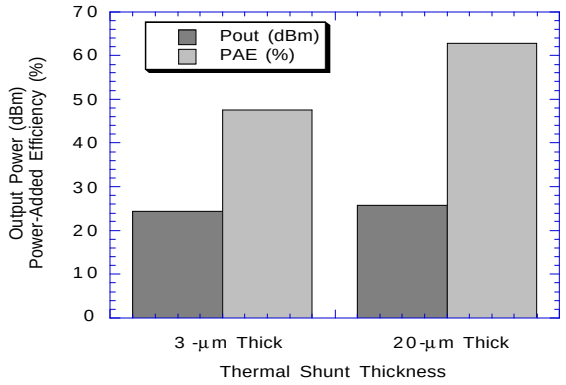

Figure 7. Comparison of output power and power-added efficiency as a function of thermal shunt thickness.

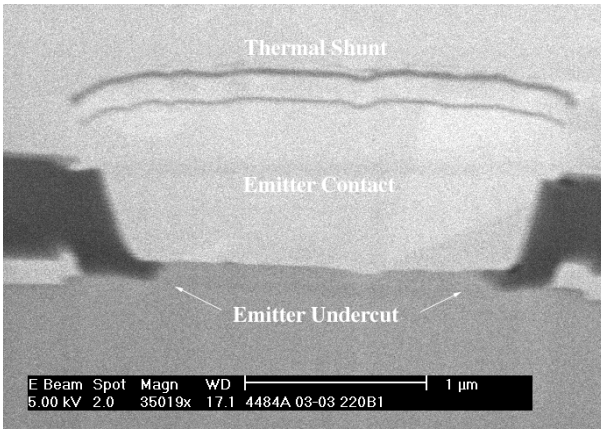

Figure 8. Focused-ion beam picture showing emitter undercut.